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Ultra-Bullet Digital Chess Clock Timer Circuit

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I. Description

The project is an Ultra-Bullet Digital Chess Clock, which is a two-player sequential countdown timer that is designed with a counter, register, and combinational logic blocks. The circuit provides each player with a single-digit countdown timer intended for extremely short chess time controls. During operation, only the timer of the player whose turn is currently active is allowed to count, while the opposing player's timer remains paused. Once a player completes a turn, the active state is then transferred to the opponent, causing the previously active timer to stop and the opponent's timer to begin counting.

The circuit can be divided into four major functional sections: the clock generator, the player-state register, the countdown counters, and the display.

An NE555 timer IC configured in astable mode serves as the common clock source. The timing resistors and capacitor connected to the NE555 determine the oscillation frequency. The oscillator is intended to generate approximately 1 Hz, such that one clock pulse corresponds to approximately one second of elapsed playing time. The generated clock is supplied to the combinational control circuitry rather than allowing both player counters to count simultaneously.

A 74LS74 dual D-type flip-flop functions as the state register of the circuit. The stored state represents which player's timer is currently active. One state enables Player 1's countdown while disabling Player 2's countdown, whereas the complementary state performs the opposite operation. Player input changes the stored state at the end of a turn. Since a flip-flop retains its output until another valid transition occurs, the circuit remembers which player is active between clock pulses. This satisfies the register or memory requirement of the sequential circuit.

The 74LS08 two-input AND gates form the principal combinational logic section. The control state from the 74LS74 is combined with the clock signal so that clock pulses are directed only toward the appropriate counter.

Each player is provided with a 74LS192 synchronous BCD up/down counter. For countdown operation, the counter decreases its four-bit BCD output for every valid clock event received while that player is active. The single-digit implementation permits the timer to

represent decimal values from 9 through 0, making the circuit suitable as a simplified ultra-bullet chess timer. The player-turn inputs are implemented as a mechanical pushbutton wired directly to the clock input of the 74LS74 flip-flop.

The BCD outputs of each 74LS192 are connected to a 74LS47 BCD-to-seven-segment decoder/driver, which translates the four-bit BCD value into the seven signals required by a common-anode seven-segment display. The displays therefore provide a direct visual indication of each player's remaining time. An active buzzer provides an audible indication associated with the expiration or terminal condition of a player's timer.

The project considers five major design constraints to ensure reliable operation of the circuit.

- Clock frequency and timing accuracy
- Logic fan-out and driving capacity
- Seven-segment display driving and current limitation
- Propagation delay and timing compatibility
- Power-supply voltage and current capacity.

Circuit Logic and Operational Specifications

To satisfy standard Low-Power Schottky Transistor-Transistor Logic (74LS TTL) operating parameters and guarantee stable timing performance, the circuit adheres to the following logic and operational specifications:

1. Power Supply Voltages

- Nominal Operating Supply (V_{CC}): 5.0 V DC
- Allowable Voltage Tolerance: 4.75 V to 5.25 V ($\pm 5\%$)
- Absolute Maximum Supply Limit: 7.0 V (operation at 6.0 V or higher risks standard IC degradation)

2. TTL Voltage Logic Levels

- Input High Voltage ($V_{IH(min)}$): 2.0 V (minimum voltage recognized as logic HIGH)
- Input Low Voltage ($V_{IL(max)}$): 0.8 V (maximum voltage recognized as logic LOW)
- Output High Voltage ($V_{OH(min)}$): 2.7 V typical under rated output current
- Output Low Voltage ($V_{OL(max)}$): 0.5 V (0.4 V typical at $I_{OL} = 10 \text{ mA}$)

3. Noise Margins

The noise immunity thresholds for the 74LS integrated circuits are established as:

- High-Level Noise Margin (NM_H):

$$NM_H = V_{OH(min)} - V_{IH(min)} = 2.7 \text{ V} - 2.0 \text{ V} = 0.7 \text{ V}$$

- Low-Level Noise Margin (NM_L):

$$NM_L = V_{IL(max)} - V_{OL(max)} = 0.8 \text{ V} - 0.5 \text{ V} = 0.3 \text{ V}$$

These noise margins ensure that spurious voltage spikes up to 0.3 V in the LOW state or 0.7 V in the HIGH state will not cause false state transitions.

4. Logic Fan-In and Fan-Out

- Logic Gate Fan-In: The 74LS08 AND gate inputs present a standard 74LS fan-in load of 1 unit load ($I_{IH} = 20\mu A$, $I_{IL} = -0.4\text{ mA}$) per input pin.
- Logic Driving Fan-Out: The 74LS08 AND gates possess a maximum driving fan-out capability of $N = 20$ standard 74LS loads. In this circuit, each AND gate drives a single 74LS192 counter clock pin, consuming only 5% of the available output drive capacity.

5. Operating Speed and Frequency

- Target Operating Frequency (f_{CLK}): 1.0 Hz ($T = 1.0\text{ s}$ per clock pulse)
- Maximum Component Toggle Frequency: 25 MHz for the 74LS192 BCD counter and 33 MHz for the 74LS74 D flip-flop.

Since the system clock frequency (1.0 Hz) is negligible compared to the maximum switching speed of the ICs, circuit response time is strictly instantaneous relative to human reaction time.

The circuit diagram illustrates a 4-bit parallel adder implemented using 74LS192N, 74LS47N, 74LS48N, and 74LS08D ICs. The circuit is powered by a 5V VCC supply. It includes two 7-segment displays (LS1, LS2) and two buzzers (BUZZER 200 Hz). The circuit features a 5V VCC supply, resistors (R1-R17), capacitors (C1, C2), and switches (S1, S2).

ICs and Components:

- 74LS192N (U2, U3):** Decade counters used for adding and subtracting.
- 74LS47N (U4, U5):** BCD-to-7-segment decoders.
- 74LS48N (U7):** BCD-to-7-segment decoder.
- 74LS08D (U9):** 4-input AND gate.
- 74LS192N (U1):** Decade counter used for the initial value.
- 74LS47N (U4):** BCD-to-7-segment decoder.
- 74LS48N (U7):** BCD-to-7-segment decoder.
- 74LS08D (U9):** 4-input AND gate.

Connections:

- Power:** VCC (5V) and GND are connected to the appropriate pins of all ICs.
- Resistors:** R1 (1kΩ), R2 (71.5kΩ), R3 (10kΩ), R4 (270Ω), R5 (270Ω), R6 (270Ω), R7 (270Ω), R8 (270Ω), R9 (270Ω), R10 (270Ω), R14 (270Ω), R15 (270Ω), R16 (270Ω), R17 (270Ω).
- Capacitors:** C1 (10μF), C2 (100nF).
- Switches:** S1 (Key = Space), S2 (Key = A).
- 7-segment Displays:** LS1 and LS2 are connected to the outputs of the decoders (U4, U5, U7) through current-limiting resistors (R4, R5, R6, R7, R8, R9, R10, R14, R15, R16, R17).
- Buzzers:** BUZZER 200 Hz are connected to the outputs of the decoders (U4, U5, U7) through current-limiting resistors (R4, R5, R6, R7, R8, R9, R10, R14, R15, R16, R17).

Figure 2.1: Complete Schematic Diagram of the Ultra-Bullet Digital Chess Clock Circuit

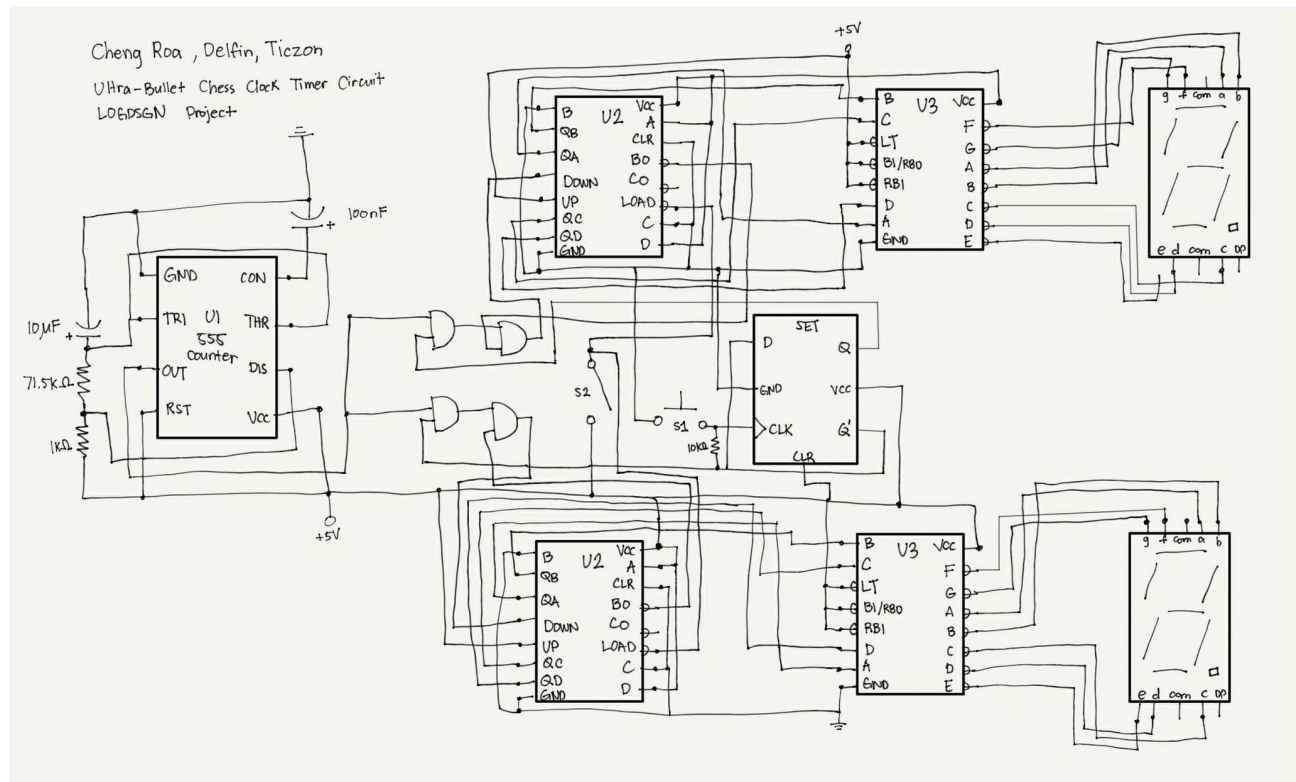


Figure 2.2: Complete Block Diagram of the Ultra-Bullet Digital Chess Clock Circuit

III. Calculations

A. Clock Generator Calculations (NE555 Astable Multivibrator)

The clock source uses an NE555 timer IC configured in astable mode to produce a nominal output frequency of $f \approx 1.0 \text{ Hz}$ (period $T \approx 1.0 \text{ s}$). The timing components consist of resistors R_1 , R_2 , and timing capacitor C_1 .

Astable Timing Equations

The charge time (output HIGH, t_{high}) and discharge time (output LOW, t_{low}) are calculated as:

$$t_{high} = \ln(2) \cdot (R_1 + R_2) \cdot C_1 \approx 0.693 \cdot (R_1 + R_2) \cdot C_1$$

$$t_{low} = \ln(2) \cdot R_2 \cdot C_1 \approx 0.693 \cdot R_2 \cdot C_1$$

The total period T and frequency f are given by:

$$T = t_{high} + t_{low} = 0.693 \cdot (R_1 + 2R_2) \cdot C_1$$

$$f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) \cdot C_1}$$

$$\text{Duty Cycle}(D) = \frac{t_{high}}{T} \times 100\% = \frac{R_1 + R_2}{R_1 + 2R_2} \times 100\%$$

Component Value Selection

To achieve $T = 1.0 \text{ s}$ using a standard capacitor value $C_1 = 10 \mu\text{F}$:

$$R_1 + 2R_2 = \frac{1.44}{f \cdot C_1} = \frac{1.44}{(1.0 \text{ Hz})(10 \times 10^{-6} \text{ F})} = 144 \text{ k}\Omega$$

Setting $R_1 = 1.0 \text{ k}\Omega$ to minimize power consumption during capacitor discharge while protecting pin 7:

$$2R_2 = 144 \text{ k}\Omega - 1.0 \text{ k}\Omega = 143 \text{ k}\Omega \rightarrow R_2 = 71.5 \text{ k}\Omega$$

Using a standard fixed resistor $R_2 = 68 \text{ k}\Omega$ in series with a $10 \text{ k}\Omega$ potentiometer set to $3.5 \text{ k}\Omega$ ($R_2 = 71.5 \text{ k}\Omega$):

$$t_{high} = 0.693 \times (1.0 \text{ k}\Omega + 71.5 \text{ k}\Omega) \times 10 \mu\text{F} = 0.502 \text{ s}$$

$$t_{low} = 0.693 \times (71.5 \text{ k}\Omega) \times 10 \mu\text{F} = 0.495 \text{ s}$$

$$T = 0.502 \text{ s} + 0.495 \text{ s} = 0.997 \text{ s} \approx 1.00 \text{ s}$$

$$f = \frac{1}{0.997\text{ s}} = 1.003\text{ Hz}$$

$$D = \frac{1\text{ k}\Omega + 71.5\text{ k}\Omega}{1\text{ k}\Omega + 2(71.5\text{ k}\Omega)} \times 100\% = 50.35\%$$

B. Player-State Register (74LS74 D Flip-Flop)

The state register maintains which player's timer is currently running. A single D Flip-Flop is configured as a toggle state machine.

State Definition

- $Q = 1$: Player 1 is Active (Timer 1 counts, Timer 2 paused)
- $Q = 0$: Player 2 is Active (Timer 2 counts, Timer 1 paused)

State Transition Diagram

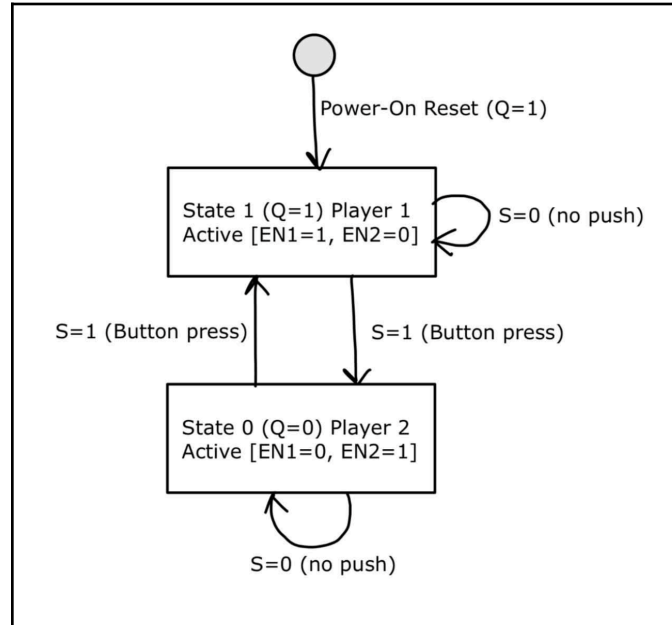


Figure 3.1: State Transition Diagram for the 74LS74 Player-State Register.

State Table

Let S represent the player turn toggle trigger input:

Present State $Q(t)$	Toggle Trigger (S)	Next State $Q(t + 1)$	Active Output State
1	0	1	Player 1 Active
1	1	0	Player 2 Active
0	0	0	Player 2 Active
0	1	1	Player 1 Active

Excitation Table

For a D Flip-Flop where $Q(t + 1) = D$:

Present State $Q(t)$	Next State $Q(t + 1)$	Required D Input	Transition Type
0	0	0	No Change (P2 holds)
0	1	1	Toggle (P2→P1)
1	0	0	Toggle (P1→P2)
1	1	1	No Change (P1 holds)

Characteristic Equation

$$Q(t + 1) = D = \overline{Q}(t)$$

Connecting the inverted output $\overline{Q}$ back to the data input D causes the flip-flop to toggle state on each valid clock pulse triggered by the player button.

C. Combinational Logic & Gating Simplification

The 74LS08 AND gates combine the 1 Hz clock signal with the state register outputs to direct clock pulses exclusively to the active counter.

Clock Routing Logic Equations

- Player 1 Gated Clock: $CLK_1 = CLK \cdot Q$
- Player 2 Gated Clock: $CLK_2 = CLK \cdot \bar{Q}$

Terminal Count & Alarm Logic Equations

The 74LS192 counter counts down from 9 (1001_2) to 0 (0000_2). When the active player reaches 0 ($Q_D Q_C Q_B Q_A = 0000_2$), the Zero Detection logic signal Z is:

$$Z = \overline{Q_D + Q_C + Q_B + Q_A} = \bar{Q}_D \cdot \bar{Q}_C \cdot \bar{Q}_B \cdot \bar{Q}_A$$

The active buzzer trigger condition B for each player simplifies to:

$$B_1 = Z_1 \cdot Q \cdot CLK$$

$$B_2 = Z_2 \cdot \bar{Q} \cdot CLK$$

D. Seven-Segment Display Current Limitation

The 74LS47 decoder drives common-anode seven-segment displays. To prevent damage to the display LEDs and stay within the 74LS47 maximum output sink current specification ($I_{OL(max)} = 24 \text{ mA}$), current-limiting resistors R_{seg} are calculated for each segment.

Parameter Specifications

- Supply Voltage: $V_{CC} = 5.0 \text{ V}$
- Segment LED Forward Voltage Drop: $V_F \approx 2.0 \text{ V}$
- 74LS47 Output Low Voltage: $V_{OL} \approx 0.4 \text{ V}$ at $I_{OL} = 10 \text{ mA}$
- Recommended Segment Forward Current: $I_F = 10 \text{ mA}$

Resistor Value Calculation

$$R_{seg} = \frac{V_{CC} - V_F - V_{OL}}{I_F} = \frac{5.0\text{ V} - 2.0\text{ V} - 0.4\text{ V}}{0.010\text{ A}} = \frac{2.6\text{ V}}{0.010\text{ A}} = 260\Omega$$

Selecting standard resistor value $R_{seg} = 270\ \Omega$ (or $330\ \Omega$):

$$I_F = \frac{2.6\text{ V}}{270\ \Omega} = 9.63\text{ mA}$$

Resistor Power Dissipation Calculation

$$P_R = I_F^2 \cdot R_{seg} = (0.00963\text{ A})^2 \times 270\ \Omega = 0.025\text{ W} = 25\text{ mW}$$

Since $25\text{ mW} \ll 250\text{ mW}$ ($1/4\text{ W}$ resistor rating), standard $1/4\text{ W}$ carbon film resistors operate well within safety margins.

E. Logic Fan-Out & Propagation Delay Compatibility

Fan-Out Calculations

For 74LS series TTL logic:

- 74LS08 Output Drive Capacity: $I_{OH(max)} = -400\ \mu\text{A}$, $I_{OL(max)} = 8\text{ mA}$
- 74LS192 Input Load Current: $I_{IH(max)} = 20\ \mu\text{A}$, $I_{IL(max)} = -0.4\text{ mA}$

$$HIGH - Level\ Fan - Out(N_H) = \frac{|I_{OH(max)}|}{I_{IH(max)}} = \frac{400\ \mu\text{A}}{20\ \mu\text{A}} = 20\text{ loads}$$

$$LOW - Level\ Fan - Out(N_L) = \frac{|I_{OL(max)}|}{|I_{IL(max)}|} = \frac{8.0\text{ mA}}{0.4\text{ mA}} = 20\text{ loads}$$

Each 74LS08 AND gate output drives only 1 counter input load, utilizing $1/20 = 5\%$ of available driving capacity.

Propagation Delay Check

- 74LS74 State Register: $t_{pd} \approx 25\text{ ns}$
- 74LS08 AND Gate: $t_{pd} \approx 15\text{ ns}$
- Total Maximum Propagation Path Delay: $t_{p(total)} = 25\text{ ns} + 15\text{ ns} = 40\text{ ns}$

Comparing to the 1.0 Hz system clock period ($T = 1.0\text{ s} = 1,000,000,000\text{ ns}$):

$$Timing\ Margin = \frac{1,000,000,000\text{ ns} - 40\text{ ns}}{1,000,000,000\text{ ns}} \times 100\% \approx 99.99996\%$$

The propagation delay is negligible, preventing race conditions or false triggers during clock state transitions.

F. Power Supply Current Budget

Component	Qty	Standby/Typical Current per IC	Total Section Current
NE555 Timer IC	1	3.0 mA	3.0 mA
74LS74 Dual D Flip-Flop	1	8.0 mA	8.0 mA
74LS08 Quad AND Gate	2	4.4 mA	8.8 mA
74LS192 BCD Counter	2	19.0 mA	38.0 mA
74LS47 Decoder/Driver	2	35.0 mA	70.0 mA
7-Segment Displays	2	67.4 mA	134.8 mA
Active Buzzer (5V active state)	2	60.0 mA	60.0 mA
Total Peak Operating Current (I_{total})			322.6 mA

Total Circuit Power Dissipation

$$P_{total} = V_{CC} \times I_{total} = 5.0 V \times 0.3226 A = 1.613 W$$

The maximum current draw of 322.6 mA is safely below the standard 5.0 V, 1.0 A regulated power supply capability.

G. Switch Input and Pull-Up Resistor Analysis

The player turn inputs are implemented using a mechanical pushbutton (S_1) wired in an active-LOW pull-up configuration to trigger the clock input pin terminal of the 74LS74 D-type flip-flop. A $10\text{ k}\Omega$ pull-up resistor ensures the clock pin remains at the nominal supply voltage of 5 V when the switch is open.

When the switch is opened (unpressed), current flows through the pull-up resistor into the clock input pin of the 74LS74. Taking into account the maximum high-level input current ($I_{IH} = 20\text{ }\mu\text{A}$ drawn by the TTL gate:

$$V_{IN(HIGH)} = V_{CC} - (I_{IH} \cdot R_{pull-up})$$

$$V_{IN(HIGH)} = 5.0\text{ V} - (20\mu\text{A} \cdot 10\text{k}\Omega) = 4.8\text{ V}$$

Since $V_{IN(HIGH)} = 4.8\text{ V} \geq V_{IH(MIN)} = 2.0\text{ V}$, the input voltage reliably guarantees a valid HIGH state with a noise margin of:

$$NM_H = V_{IN(HIGH)} - V_{IH(MIN)}$$

$$NM_H = 4.8\text{ V} - 2.0\text{ V} = 2.8\text{ V}$$

When the switch is closed (pressed), the input pin is pulled directly to the ground:

$$V_{IN(LOW)} = 0\text{ V}$$

Since $0\text{ V} \leq V_{IL(MAX)} = 0.8\text{ V}$, the input voltage satisfies the TTL logic LOW requirement with a noise margin of:

$$NM_L = V_{IL(MAX)} - V_{IN(LOW)}$$

$$NM_L = 0.8\text{ V} - 0\text{ V} = 0.8\text{ V}$$

IV. Data and Results

A. NE555 Astable Multivibrator Simulation

First results show the NE555 as a stable clock generator. The purpose of the simulation was to verify that the circuit produced a periodic clock signal that could serve as the timing source for the ultra-bullet digital chess clock.

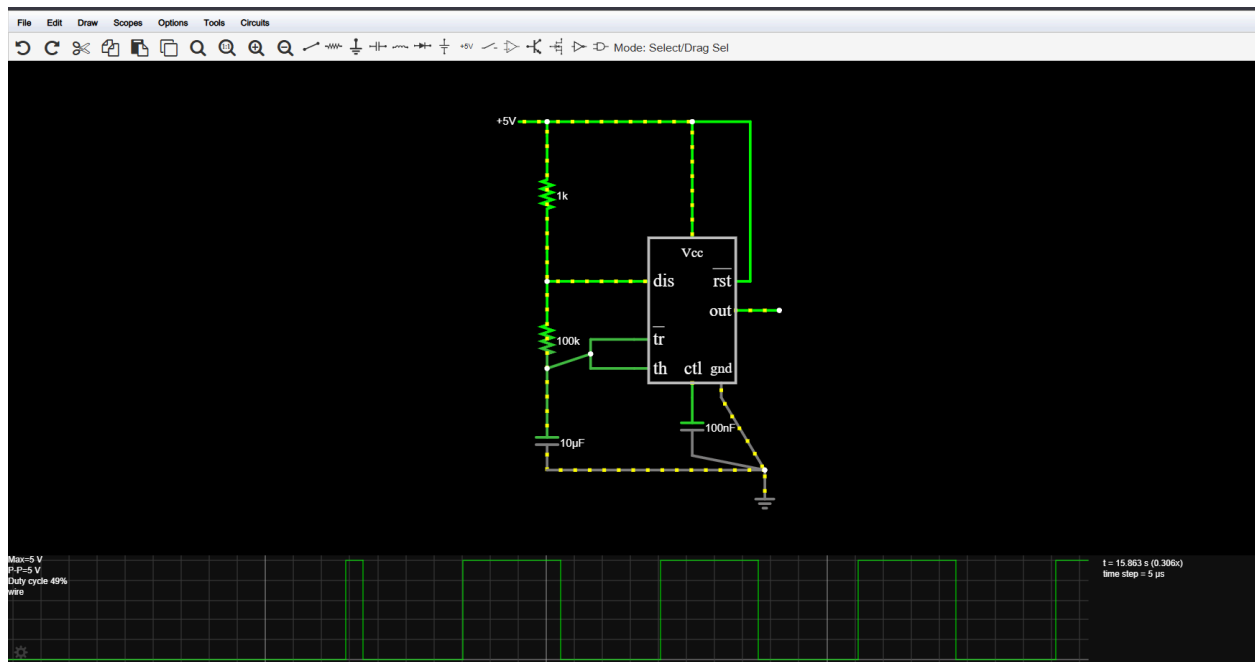


Figure 4.1: Simulated NE555 Astable Multivibrator output waveform

Figure 4.1 shows the simulated output waveform of the NE555 Astable Multivibrator. Using a 5 V supply, a 1 k Ω resistor, a 100 k Ω resistor, and a 10 μ F timing capacitor, the circuit produced a repeating square-wave output suitable for use as the clock source of the proposed chess timer. The simulated waveform reached a maximum output voltage of 5 V and a peak-to-peak voltage of 5 V. The measured duty cycle was approximately 49%, indicating that the HIGH and LOW intervals were nearly equal. This confirms that the clock generator provided a stable periodic signal to the subsequent sequential logic stages of the circuit.

Table 4.1 Ne555 Astable Multivibrator Simulation Results

Parameter	Simulated Value
Supply Voltage	5V
Resistor R1	1 k Ω
Resistor R2	100 k Ω
Capacitor C	10 μ F
Maximum Output Voltage	5V
Peak-to-Peak Voltage	5V
Duty Cycle	49%
Frequency (approx)	0.716 Hz
Period	1.396s

B. Player-State Register (74LS74 D Flip-Flop)

The player-state register was simulated using a D flip-flop configured in toggle mode by connecting the complemented output $\bar{Q}$ back to the input D. The purpose of the simulation was to verify that the active-player state alternates whenever a valid rising-edge input pulse is applied. Based on the circuit definition, $Q=1$ represents Player 1 as active, while $Q=0$ represents Player 2 as active.

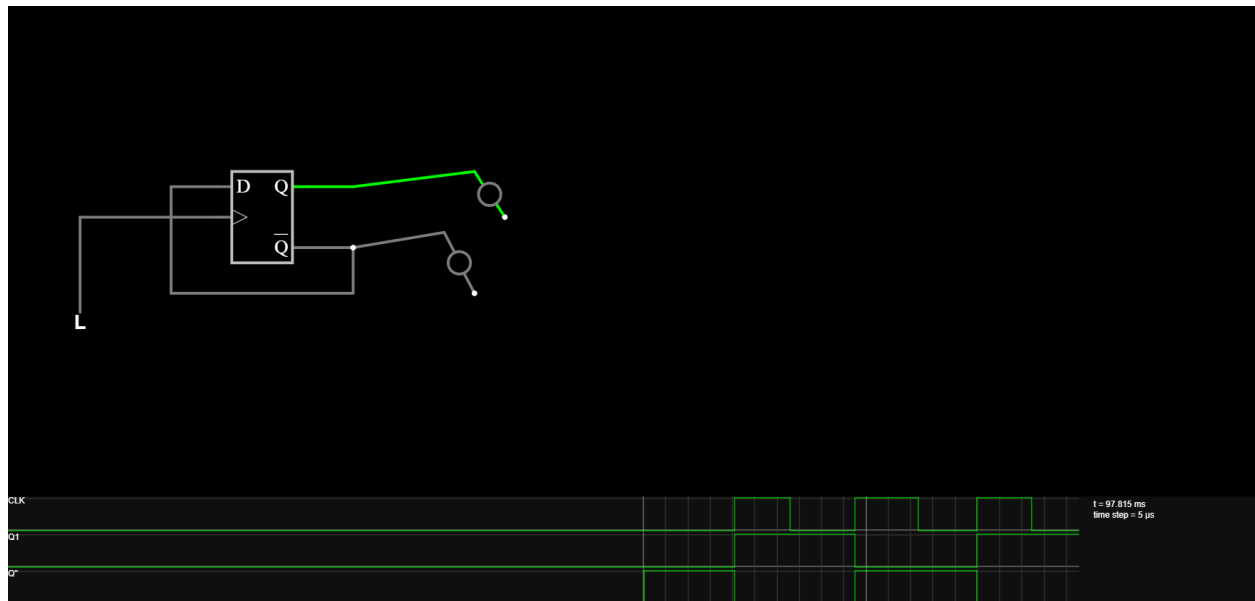


Figure 4.2: Simulated timing diagram of the player-state register.

Figure 4.2 shows the simulated timing behavior of the player-state register. The D flip-flop was configured so that Q is fed back to the D input, causing the stored state to toggle on every rising edge of the clock input. During the initial state, $Q=1$ and $Q=0$, corresponding to Player 1 being active. After the first rising edge, the outputs changed to $Q=0$ and $Q=1$, transferring the active state to Player 2. Succeeding rising edges continued to alternate the active state between the two players. The simulation therefore confirms that the player-state register performs the required turn-switching function of the digital chess clock.

Table 4.2 Player-State Register Simulation Results

Test Condition	Input Transition	Q	Q'	Active Player
Initial State	L	1	0	Player 1
1st Rising Edge	L → H	0	1	Player 2
2nd Rising Edge	L → H	1	0	Player 1
3rd Rising Edge	L → H	0	1	Player 2

C. Clock Routing and Gating Simulation

The clock-routing circuit was simulated to verify that the system clock is delivered only to the counter of the active player. Two AND gates were used to combine the system clock with the player-state outputs. The Player 1 gated clock is represented by $CLK1 = CLK \cdot Q$, while the Player 2 gated clock is represented by $CLK2 = CLK \cdot Q'$.

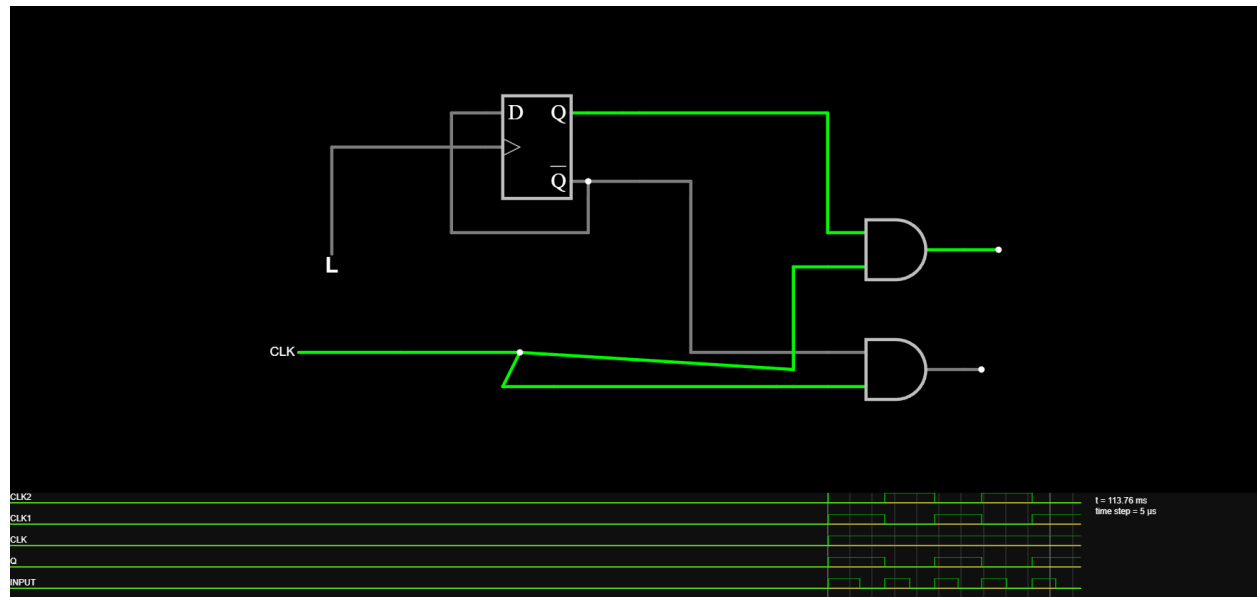
**Figure 4.3:** Simulated timing diagram of the clock-routing and gating circuit.

Figure 4.3 shows the simulated operation of the clock-routing logic. When $Q=1$, corresponding to Player 1 being active, the first AND gate allows the system clock to pass through as $CLK1$, while $CLK2$ remains LOW. When the player-state register changes to $Q=0$, the first gated clock is disabled, and $CLK2$ follows the system clock through the second AND

gate. The simulation confirms that clock pulses are directed exclusively to the active player's timer, preventing both countdown counters from operating simultaneously.

Table 4.3 Clock Routing and Gating Simulation Results

Player State	Q	Q'	CLK1	CLK2
Player 1 Active	1	0	Follows CLK	LOW
Player 2 Active	0	1	LOW	Follows CLK

D. Up/Down Counter and Seven-Segment Display Simulation

The countdown and display section was simulated to verify the operation of the counter and its corresponding seven-segment output. A functional four-bit up/down counter was connected to a seven-segment decoder and display in Falstad to represent the operation of the 74LS192 counter and 74LS47 decoder used in the proposed circuit. The counter direction was controlled through the U/D input. During testing, a LOW U/D input resulted in upward counting, while a HIGH U/D input resulted in downward counting.

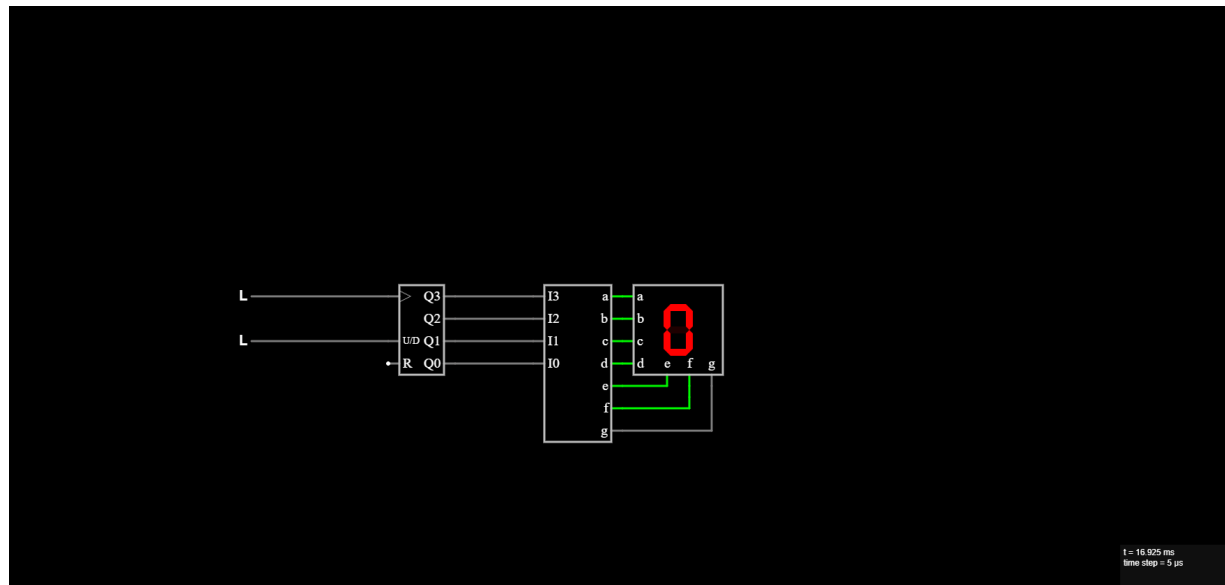


Figure 4.4A: Initial counter and seven-segment display state at 0.

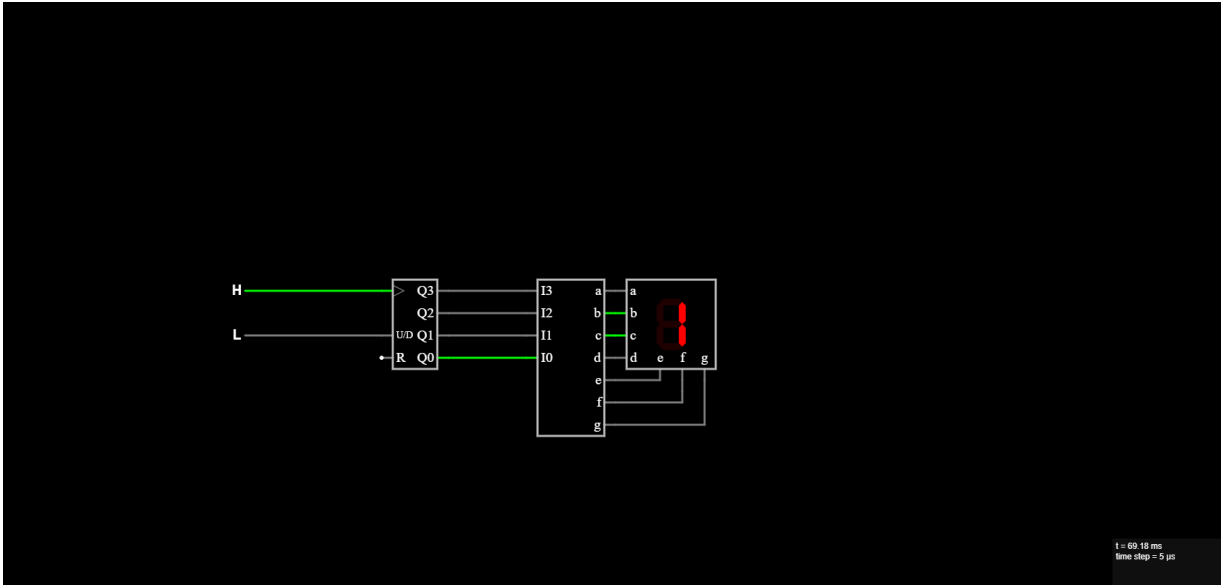


Figure 4.4B: Up-count operation from 0 to 1 with U/D set LOW.

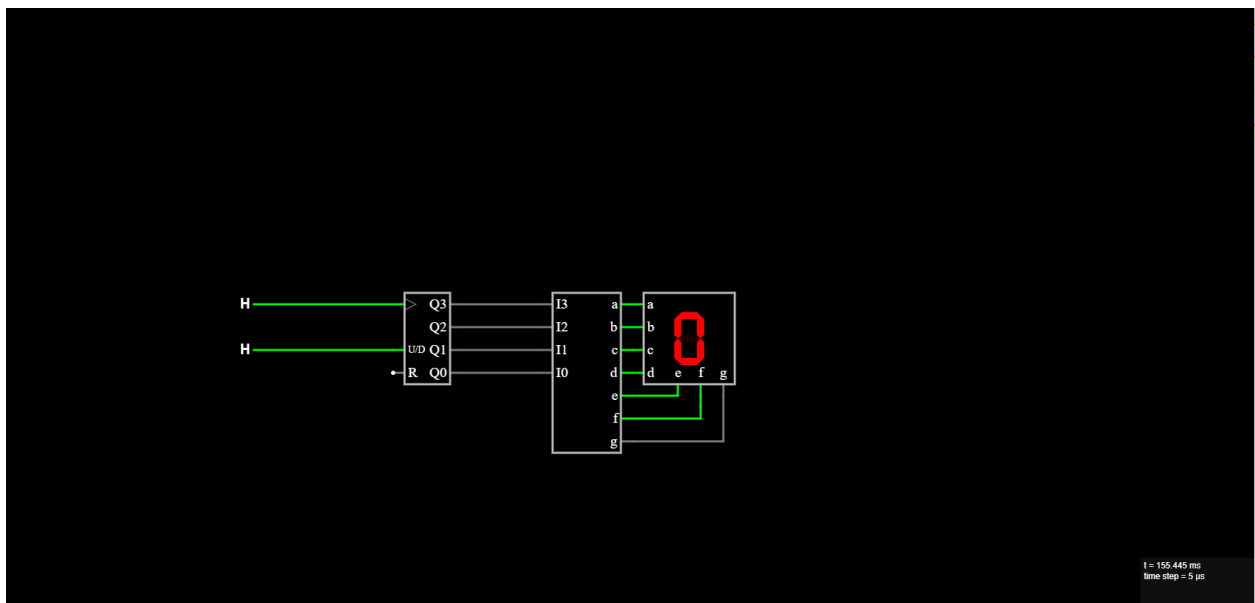


Figure 4.4C: Counter direction changed to DOWN with U/D set HIGH while the displayed value remains at 0.

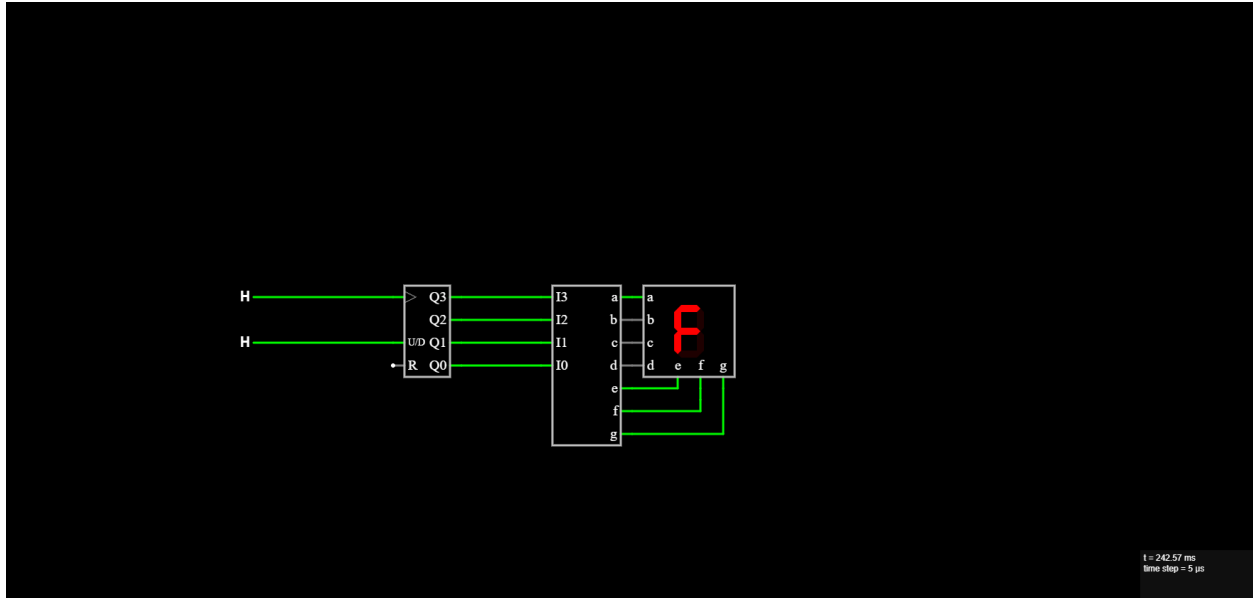


Figure 4.4D: Generic four-bit counter wraparound from 0 to 1111, displayed as F, during downward counting.

Figures 4.4A to 4.4D show the simulated behavior of the counter and seven-segment display subsystem. In Figure 4.4A, the counter begins at the binary state 0000, which is decoded and displayed as 0. With the U/D control set LOW, a valid clock transition increments the counter to 0001, producing the decimal digit 1 as shown in Figure 4.4B. Changing U/D to HIGH selects the downward-counting direction; however, changing the direction input alone does not alter the stored counter value, as demonstrated in Figure 4.4C. When another clock transition is applied while counting downward from zero, the generic four-bit Falstad counter wraps to 1111, which is displayed as F in Figure 4.4D. This confirms the operation of the direction-control input, clock-driven counting, binary output, decoder, and seven-segment display path.

The Falstad simulation uses a generic four-bit up/down counter rather than an exact 74LS192 BCD counter model. Consequently, the simulated counter can enter binary states above 1001 and wrap from 0000 to 1111 during downward counting. In the proposed hardware circuit, the 74LS192 operates as a BCD counter and is intended to represent the decimal countdown range from 9 to 0.

Table 4.4 Up/Down Counter and Seven-Segment Display Simulation Results

Figure/Test	Clock/Input Condition	U/D	Counter Output	Display	Observation
Figure 4.4A	Initial state	LOW	0000	0	Counter begins at zero
Figure 4.4B	Rising clock transition	LOW	0001	1	Counter increments from 0 to 1
Figure 4.4C	Direction changed	HIGH	0000	0	U/D selects downward counting; changing direction alone does not change the count
Figure 4.4D	Down-count clock transition from 0	HIGH	1111	F	Generic Falstad counter wraps from 0 to 15

E. Terminal Count and Alarm Simulation

The terminal-count detection and alarm section was simulated to verify that the alarm activates only when the counter reaches zero. A zero-detection logic circuit was implemented using two OR gates and one NOR gate connected to the four counter outputs. The outputs Q3 and Q2 were combined by the first OR gate, while Q1 and Q0 were combined by the second OR gate. The outputs of the two OR gates were then applied to a NOR gate to generate the terminal-count signal. When the counter value is 0000, the NOR output becomes HIGH, activating the alarm indicator. For all other counter values, the alarm output remains LOW.

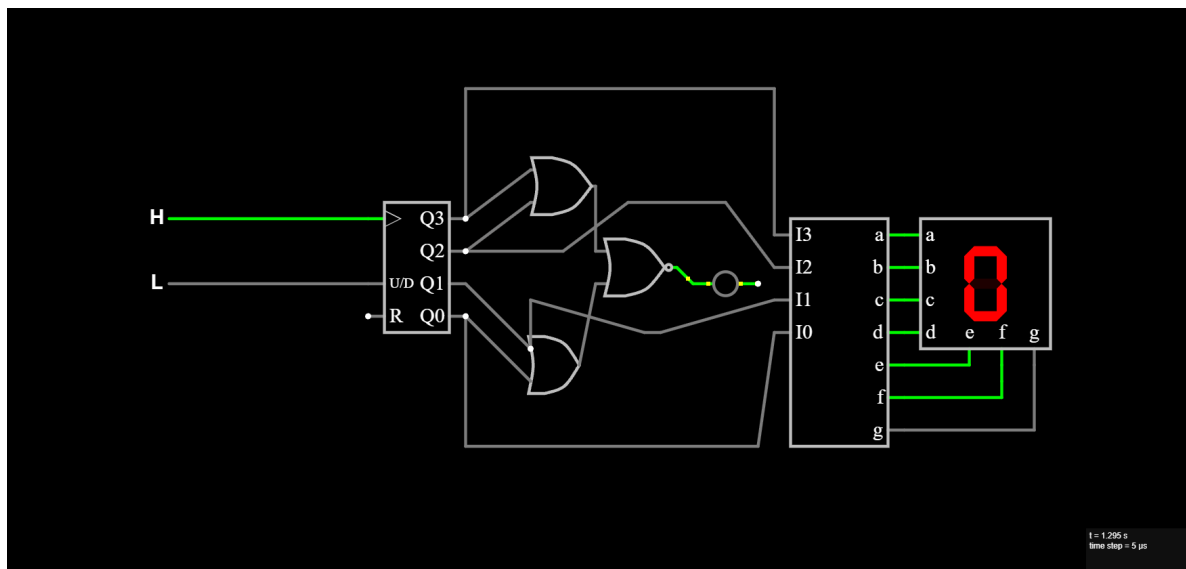


Figure 4.5A: Terminal-count condition at 0 with alarm output activated.

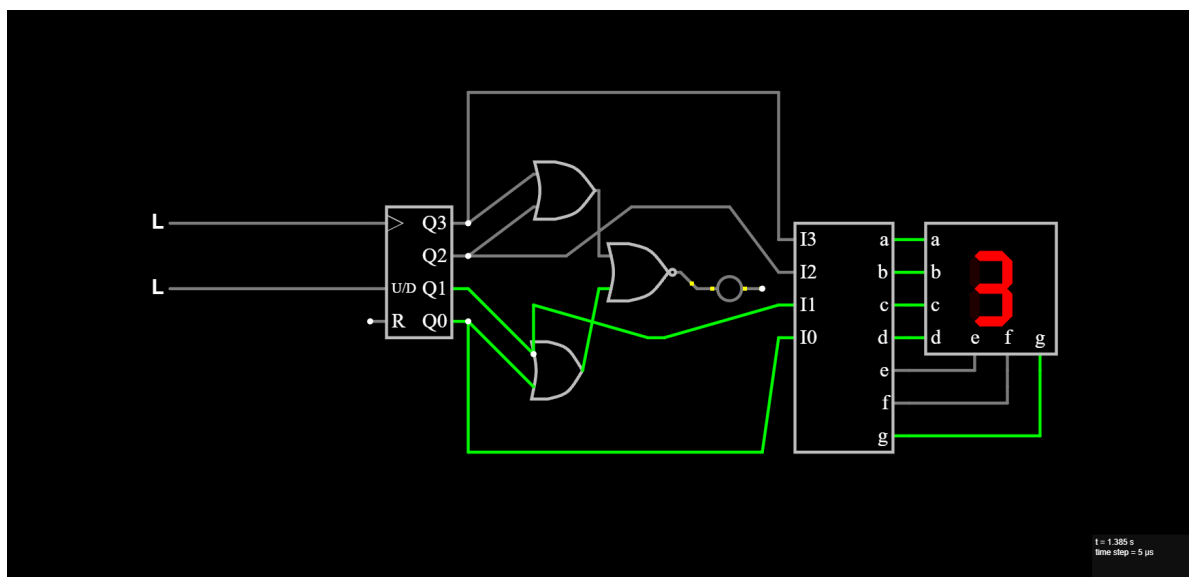


Figure 4.5B: Non-terminal counter state at 3 with alarm output deactivated.

Figures 4.5A and 4.5B demonstrate the operation of the terminal-count detection circuit. In Figure 4.5A, the counter output is 0000, corresponding to a displayed value of 0. Since all four counter outputs are LOW, the NOR-based zero-detection circuit produces a HIGH output, activating the alarm indicator. In Figure 4.5B, the counter output corresponds to decimal 3 (0011); because the counter is no longer at zero, the zero-detection output becomes LOW, and the alarm remains inactive. These results confirm that the alarm is activated only when the counter reaches its terminal value of zero.

Table 4.5 Terminal Count and Alarm Simulation Results

Figure/Test	Clock Input	U/D Input	Counter Output	Display	Alarm Output	Observation
Figure 4.5A	HIGH	LOW	0000	0	HIGH / ON	Terminal count detected; alarm activates at zero
Figure 4.5B	LOW	LOW	0011	3	LOW / OFF	Counter is above zero; alarm remains inactive

F. Integrated Multisim Circuit Validation

The complete Ultra-Bullet Digital Chess Clock circuit was built and simulated in Multisim to validate the operation of the individual subsystems when interconnected as a complete system. Unlike the preceding functional simulations, the integrated Multisim model utilized the specified LM555CN timer, 74LS74 D flip-flop, 74LS08 logic gates, 74LS192 counters, 74LS47 decoder/drivers, and seven-segment displays. Oscilloscope and multimeter probes were used to obtain the actual clock waveform, TTL voltage levels, state-register outputs, and gated clock signals. The measured values were then compared with the theoretical design values to evaluate the overall operation of the circuit.

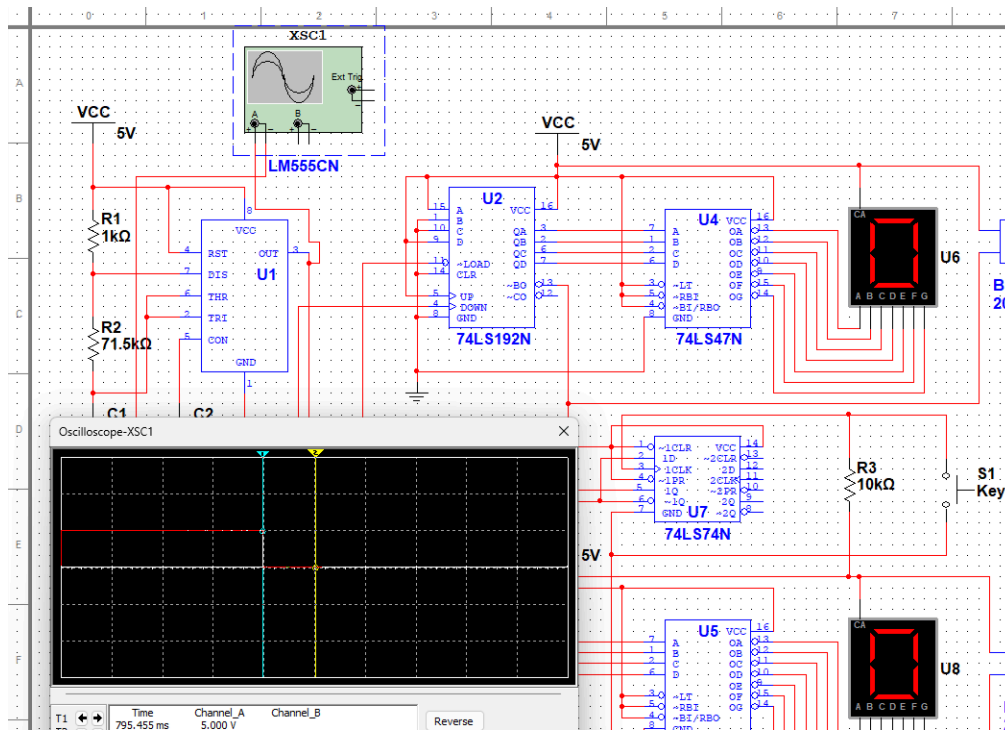


Figure 4.6A: Multisim oscilloscope HIGH TIME measurement of the LM555CN clock output.

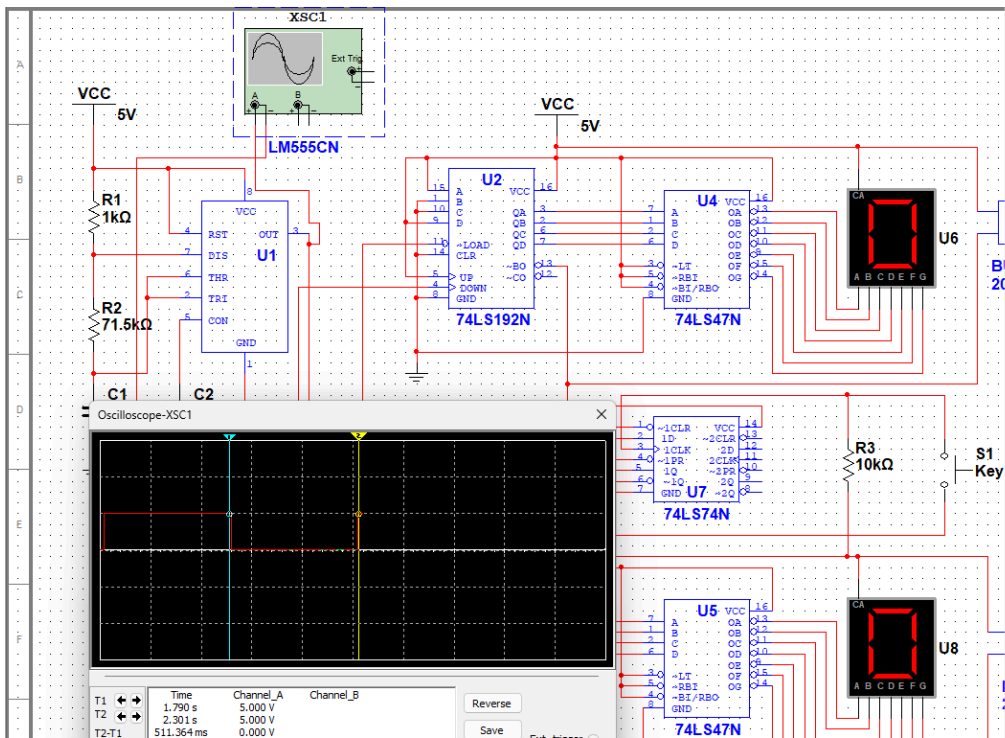


Figure 4.6B: Multisim oscilloscope LOW TIME measurement of the LM555CN clock output.

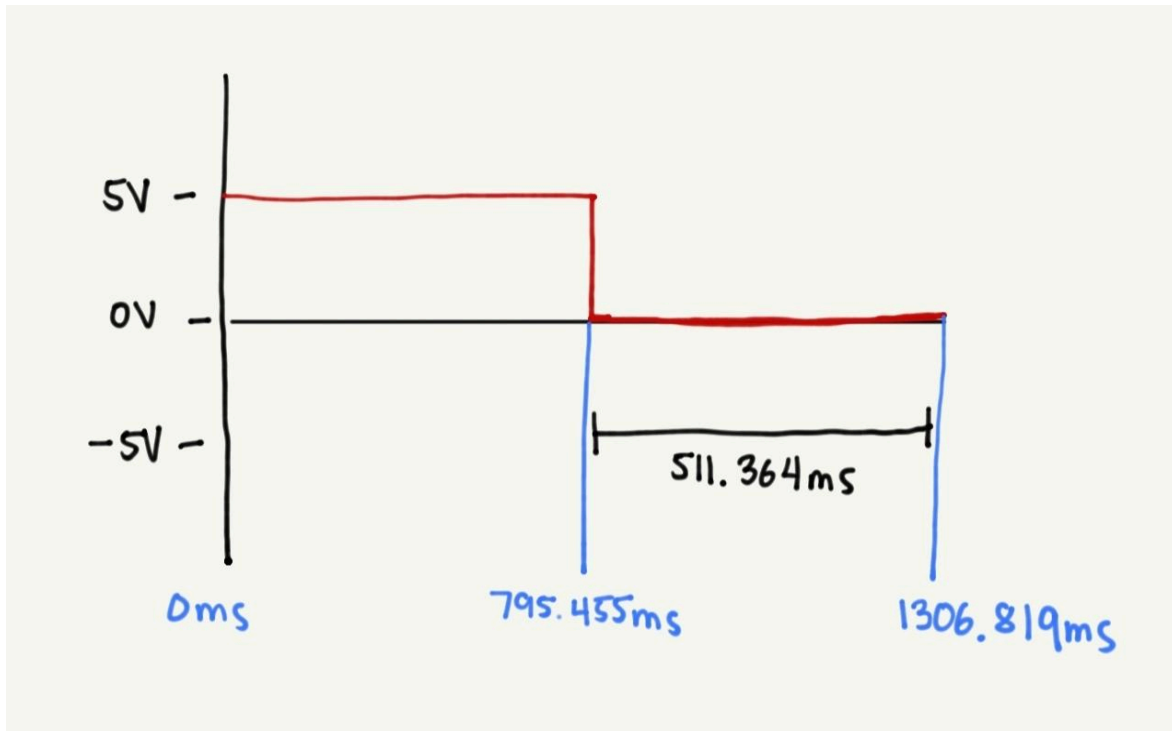


Figure 4.7: Measured HIGH and LOW intervals of the LM555CN clock waveform.

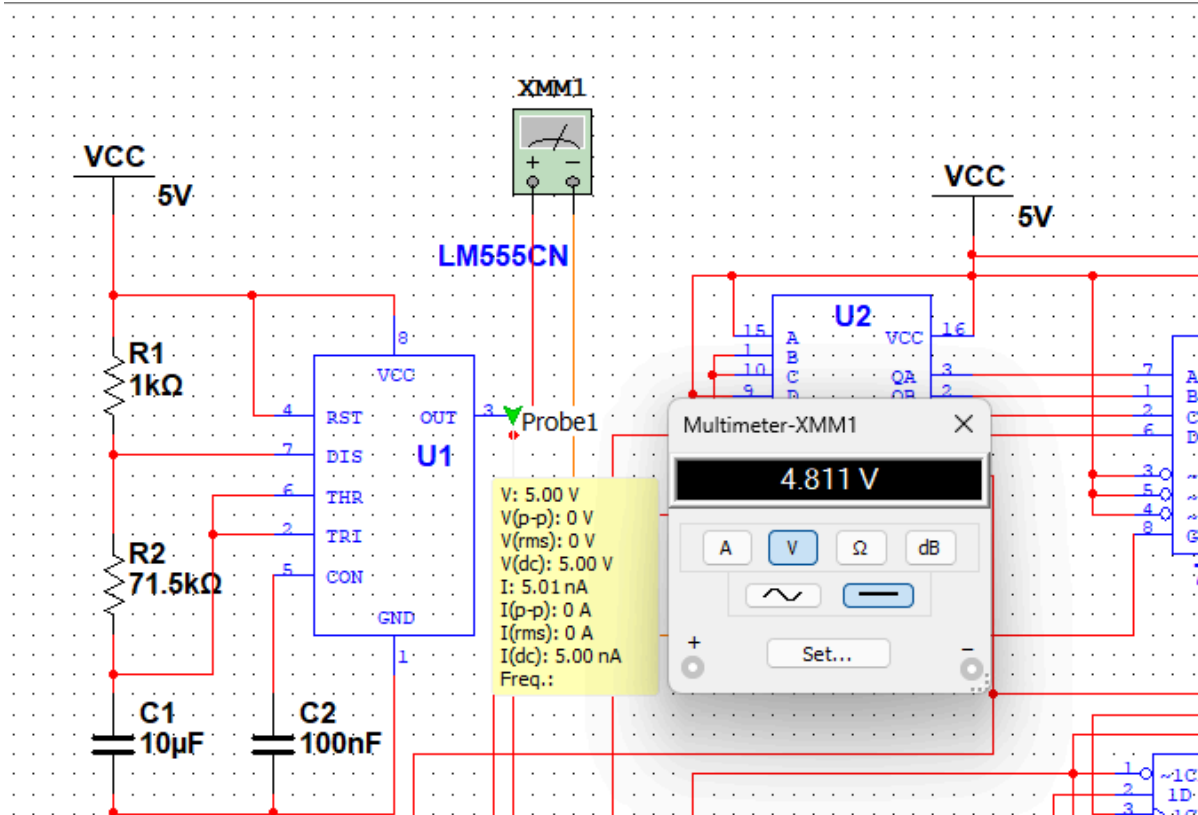


Figure 4.8A: Measured HIGH-state voltage of the LM555CN clock output.

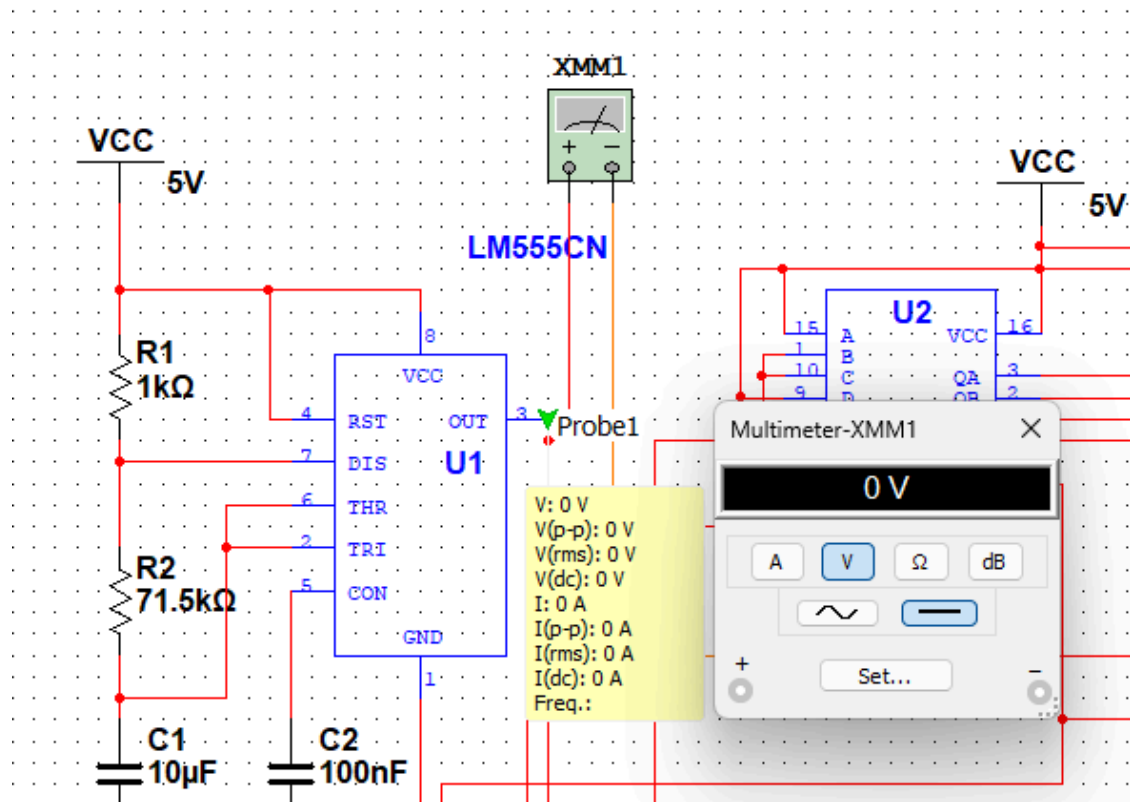


Figure 4.8B: Measured LOW-state voltage of the LM555CN clock output.

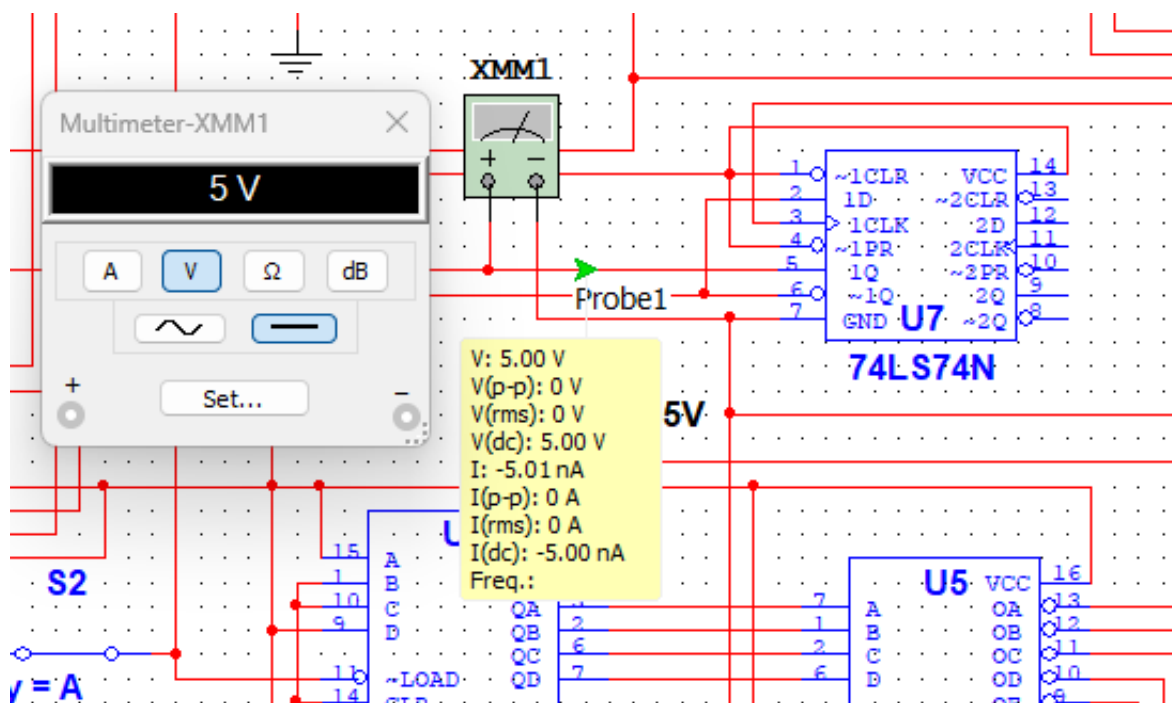


Figure 4.8C: Measured HIGH-state output of the 74LS74 player-state register.

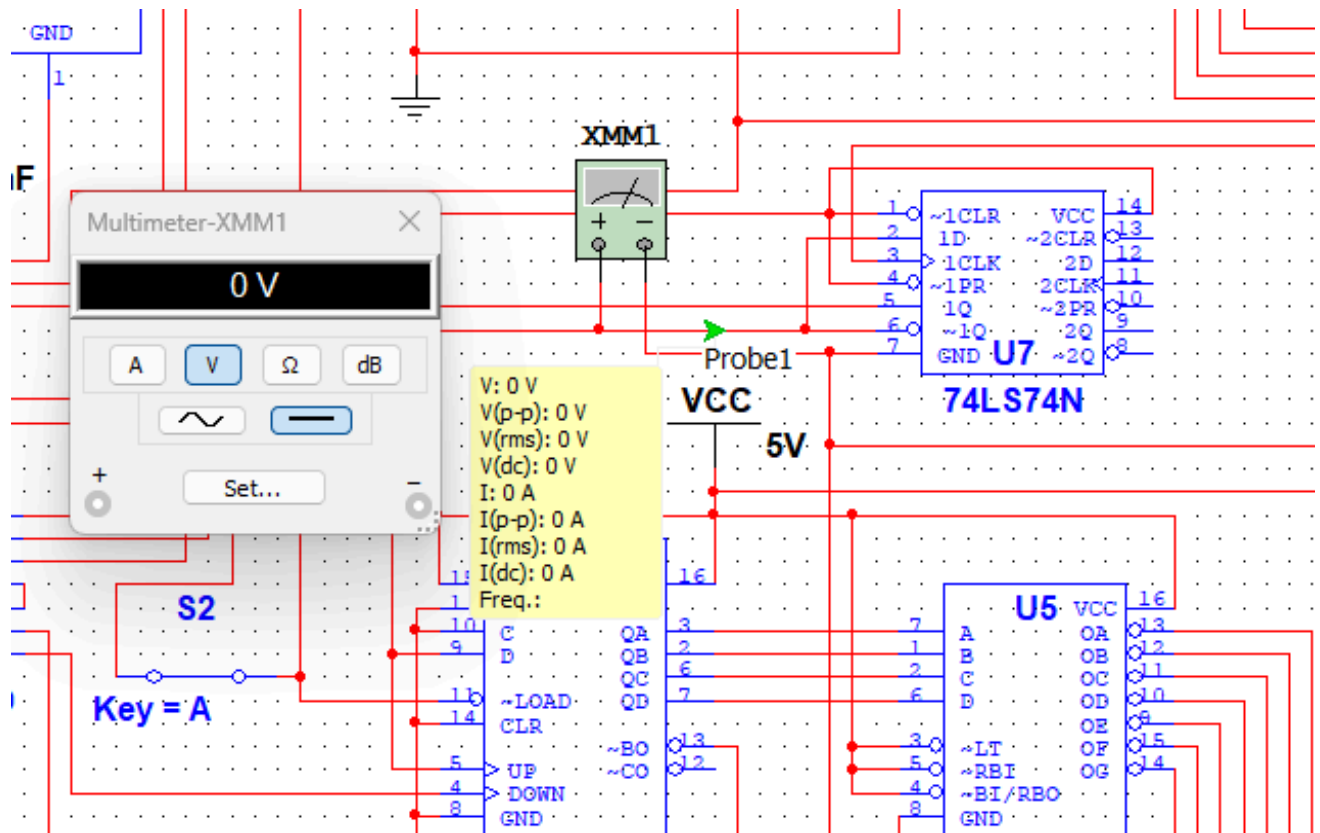


Figure 4.8D: Measured LOW-state output of the 74LS74 player-state register.

F.1 LM555 Clock Generator — Integrated Results

The integrated LM555CN simulation produced a stable periodic output between approximately 0 V and 4.811 V. The measured HIGH and LOW voltages satisfy the required TTL input limits and are therefore suitable for driving the succeeding logic stages. The measured period was approximately 1.30682 s, corresponding to a clock frequency of approximately 0.7652 Hz. This is lower than the theoretical design target of 1.003 Hz by approximately 23.71%. The measured duty cycle was also higher than the calculated value, increasing from the theoretical 50.35% to approximately 60.87%. Although a timing deviation was observed, the oscillator remained periodic and functioned correctly as the integrated circuit's common clock source.

Table 4.6 Integrated LM555 Clock Generator Measurement Results

Parameter	Theoretical Value	Multisim Measured Value	Percentage Error / Deviation	Status
Supply Voltage (V_{cc})	5.000 V	5.000 V	0.00%	Pass
Output High Voltage (V_{OH})	5.000 V	4.811 V	3.78%	Pass
Output Low Voltage (V_{OL})	0.000 V	0.000 V	0.00%	Pass
Peak-to-Peak Voltage (V_{p-p})	5.000 V	4.811 V	3.78%	Pass
High Time (t_{high})	502.42 ms	795.455 ms	+58.32%	Deviation noted
Low Time (t_{low})	495.50 ms	511.364 ms	+3.20%	Pass
Total Period (T)	0.997s	1.30682 s	+31.08%	Deviation noted
Clock Frequency (f) CLK	1.003 Hz	0.7652 Hz	-23.71%	Deviation noted
Duty Cycle (D)	50.35%	60.87%	+20.89%	Deviation noted

F.2 TTL Logic Levels and Noise Margins

The voltage measurements demonstrate that the integrated circuit maintains valid TTL logic levels throughout the clock-generation, state-register, and clock-routing stages. The LM555CN clock HIGH level of 4.811 V exceeds the minimum TTL HIGH requirement of 2.0 V, producing a HIGH-level noise margin of 2.811 V. Its LOW level of 0 V is also below the maximum TTL LOW threshold of 0.8 V. Similarly, the 74LS74 outputs produced approximately 5 V for the active HIGH state and 0 V for the complementary LOW state. All measured logic states therefore satisfy the required TTL thresholds with sufficient noise margins.

Table 4.7 TTL Logic-Level and Voltage-Margin Probe Results

Test Point	Operating State	Measured Voltage	TTL Requirement	Noise Margin	Status
LM555 OUT	HIGH	4.811 V	$V_{IH(min)} = 2.0V$	$NM_H = 2.811V$	Pass
LM555 OUT	LOW	0.000 V	$V_{IL(max)} = 0.8V$	$NM_L = 0.800V$	Pass
74LS74 Q	Active HIGH	5.000 V	$V_{IH(min)} = 2.0V$	$NM_H = 3.000V$	Pass
74LS74 Q'	Inactive LOW	0.000 V	$V_{IL(max)} = 0.8V$	$NM_L = 0.800V$	Pass
CLK1	Gated Active	0 - 4.811 V, 0.7652 Hz	TTL HIGH/LOW	$NM_H = 2.811V$, $NM_L = 0.800V$	Pass
CLK2	Gated Inactive	0.000 V	$V_{IL(max)} = 0.8V$	$NM_L = 0.800V$	Pass

F.3 Player-State Register and Clock Routing

The integrated simulation was verified by the interaction between the player-state register and clock-routing logic. At power-on, $Q=1$ and $Q'=0$, causing CLK1 to receive the periodic clock signal while CLK2 remains continuously LOW. After the first valid player-button transition, the flip-flop changes to $Q=0$ and $Q'=1$. Consequently, CLK1 becomes inactive, and CLK2 begins receiving the oscillator signal. Subsequent button transitions repeatedly reverse these conditions. The measured sequence confirms that only one player timer receives clock pulses at a time, while the opposing timer remains paused. This behavior satisfies the primary turn-switching requirement of the Ultra-Bullet Digital Chess Clock.

Table 4.8 Integrated Player-State Register and Clock-Routing Results

Sequence / Event	Switch S1	Present Q(t)	Next Q(t+1)	Q'	CLK1	CLK2
Power-On Initial State	Open	1	1	0	Oscillating, 0.765 Hz	Constant LOW
1st Button Trigger	L→H	1	0	1	Constant LOW	Oscillating, 0.765 Hz
2nd Button Trigger	L→H	0	1	0	Oscillating, 0.765 Hz	Constant LOW
3rd Button Trigger	L→H	1	0	1	Constant LOW	Oscillating, 0.765 Hz

Overall, the integrated Multisim results confirm that the major sections of the circuit operated together as intended. The clock generator produces a stable periodic timing signal, the 74LS74 retains and alternates the active-player state, and the clock-routing logic directs clock pulses exclusively to the selected player's counter. All measured HIGH and LOW voltages satisfy standard TTL logic requirements. Although the measured LM555 clock frequency differed from the theoretical 1 Hz design target, the functional behavior of the sequential and combinational logic remained correct.

V. Conclusion

To conclude, the desired design for the Ultra-Bullet Digital Chess Clock was successfully achieved based on the functional and integrated simulation results. The circuit was able to generate a periodic clock signal, store and alternate the active-player state, route the clock exclusively to the selected player, perform counter and seven-segment display operations, and activate the alarm when the terminal count of zero was reached. The Falstad simulations verified the behavior of the individual functional sections, while the Multisim simulation further confirmed the operation of the circuit using the specified LM555CN, 74LS74, 74LS08, 74LS192, and 74LS47 components. The measured TTL HIGH and LOW voltage levels were also within the required logic limits, indicating reliable communication between the different logic stages.

Several problems were encountered during the design and simulation process. One of the main issues was the difference between the theoretical NE555 clock frequency and the measured Multisim result. The calculated frequency was approximately 1.003 Hz, while the integrated simulation produced approximately 0.7652 Hz, together with differences in the measured HIGH time and duty cycle. Another limitation occurred in Falstad because its generic four-bit up/down counter does not behave exactly like the 74LS192 BCD counter and therefore wraps from 0000 to 1111 during downward counting. These limitations were addressed by using the Falstad simulations mainly for functional verification and the Multisim model for validation using the actual 74LS-series IC models. The terminal-count circuit was also tested separately to confirm that the alarm activates only when the counter reaches 0000.

Overall, the project demonstrated the application of sequential and combinational logic in a practical two-player timing system. Despite the observed timing deviation and simulator limitations, the essential logic functions of the design operated as intended. The project therefore satisfied its main objective of developing a simplified digital chess clock in which only the active player's timer counts, and player turns can be alternated through the state register, while the remaining count is displayed visually, and an alarm indicates expiration of the timer.

VI. Appendices

Appendix A. Distribution of Tasks

Member	Contribution
John Carlo Cheng Roa	Description (34%) Schematic Diagram/Block Diagram (100%) Calculations (10%) Data and Results (10%) Conclusion (33%)
Nirah Delfin	Description (33%) Calculations (80%) Data and Results (10%) Conclusion (33%)
Julio Luis Gabriel Ticzon	Description (33%) Calculations (10%) Data and Results (80%) Conclusion (34%)

Appendix B. Proof of Collaboration

The screenshot shows a Slack conversation thread. On the left, a message from Nirah Delfin (6:51 PM Yesterday) asks for clarification on choosing between 'one noh?' or 'do we have to do both block and schematic?'. John Carlo Cheng Roa (3:00 AM Today) responds, and the message is marked as resolved. In the center, a message from Nirah Delfin (10:14 PM Today) asks if 'LOW' should be 'insteadd ?'. John Carlo Cheng Roa (10:16 PM Today) replies 'yup, thanks for catching'. On the right, a message from Nirah Delfin (5:57 PM Yesterday) asks 'julio Show here simulation results including timing diagrams, and other test values.'. Julio Luis Gabriel Ticzon (6:03 PM Yesterday) replies 'yess'.

The screenshot shows a WhatsApp chat. Nirah Delfin sends a message: 'hello im trying to do the calculation part sa paper, lmk if its ok pa HAHA'. An unnamed contact replies: 'not yet done e'. Nirah Delfin then sends: 'thank uu!'. Another unnamed contact replies: 'don't worry, keep working on it nalang, i'll correct if may mali'.

