



De La Salle University – Manila

Term 3, 2025 - 2026

Single-Digit Random Number Circuit Design Simulation

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OBJECTIVES

1. To be able to design a digital circuit using both sequential and combinational circuits
2. To be able to implement the designed circuits on both the breadboard and PCB.
3. Create a digital dice roller circuit using different IC's.

MATERIALS

- 1x 74LS90 — Decade Counter
- 1x 74LS47 — BCD-to-7-Segment Decoder/Driver
- 1x NE555P — 555 Timer IC
- 1x Common Anode 7-Segment Display
- 4x 300 Ω resistor ($\frac{1}{4}$ W)
- 3x 10 k Ω resistor ($\frac{1}{4}$ W)
- 2x 2.5 μ F electrolytic capacitor
- 4x 5mm LED
- 1x SPST Momentary Pushbutton
- Piezo Buzzer
- Breadboard
- Male-to-male jumper wires
- 5 V regulated power supply (or USB 5 V module)

DETAILED PROJECT DESCRIPTION

The circuit simulates a random number generator using a 7-segment display and multiple digital ICs. It starts with an astable 555 timer circuit that generates rapid and continuous clock pulses as long as the button is held down. It has a rapid, high-frequency signal that then drives the 74LS90, which is incrementing in binary from 0 to 9 on each clock pulse, which can be observed by the LEDs. This is then connected to 74LS47 along with a 7-segment display to show its corresponding decimal number.

The clock signal from the 555 timer reaches pin 14 of the 74LS90 through a pushbutton, which is wired in junction with a 10k pull-down resistor (R3) connected to ground. While the button is unpressed, R3 holds pin 14 at a stable LOW logical level, preventing floating and picking up any noise that could trigger or create false outputs. Once the button is pressed, it connects the 555 oscillating output to pin 14, allowing the clock pulses to actively drive the counter. Releasing it disconnects the path, and R3 pins it to a stable LOW.

How the 74LS90 works is it increments in 10 states (0-9) in BCD (0000-1001), cycling through its full range before automatically resetting back to 0000 and repeating its sequence. This cycle only occurs when the button is pressed; however, due to the 555 timers' high frequency, these change in states goes faster than the human eye can track. Pressing the button also creates a sound cue and a visual cue to know that it's cycling. The sound cue comes from the Piezo buzzer, which beeps at short but quick intervals, while its visual cue comes from the LEDs of the output 74LS90, cycling between the binary of 0-9. Once it's released, the clock, counter, and buzzer stop, showing whichever value it has landed on, producing an output that appears random and simulating a single-digit random number generator.

The output of 74LS90 is fed into two different displays: a 7-segment display and a binary output. For each bit on the binary output, it is connected in series to an individual LED with a resistor. While for the 7-segment display it's a common-anode, which is connected to a 74LS47, which converts the BCD output into the correct combination of illuminated segments to display the corresponding digit of 0-9.

SCHEMATIC DIAGRAM

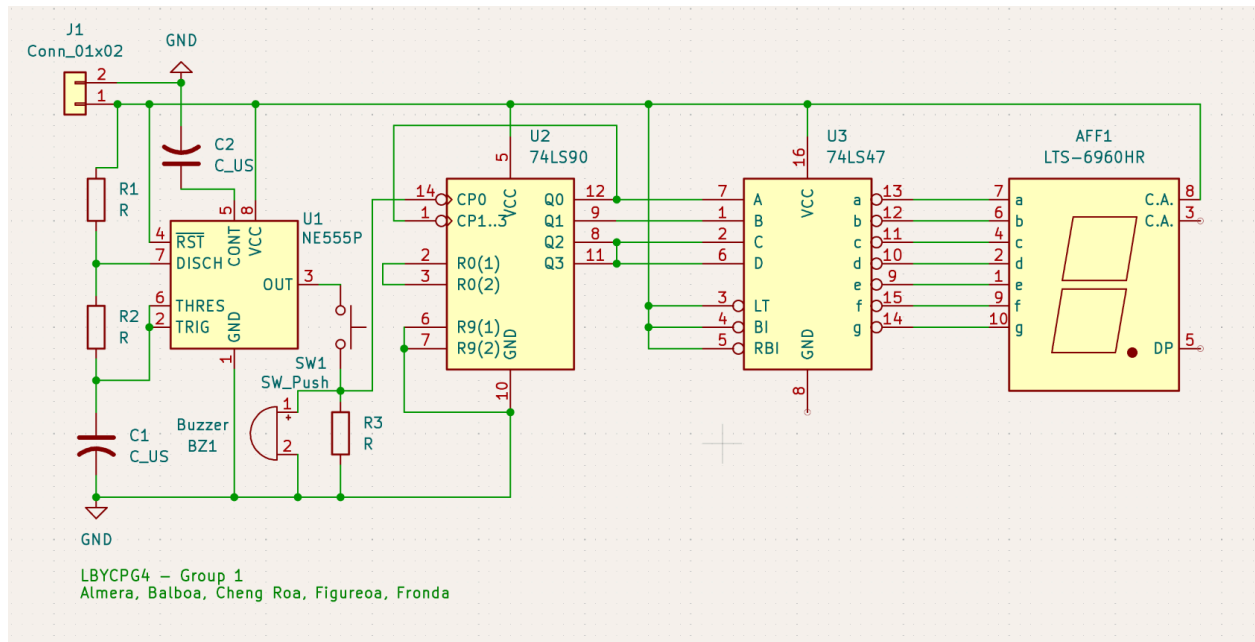


Figure 1. Schematic Diagram using KiCad

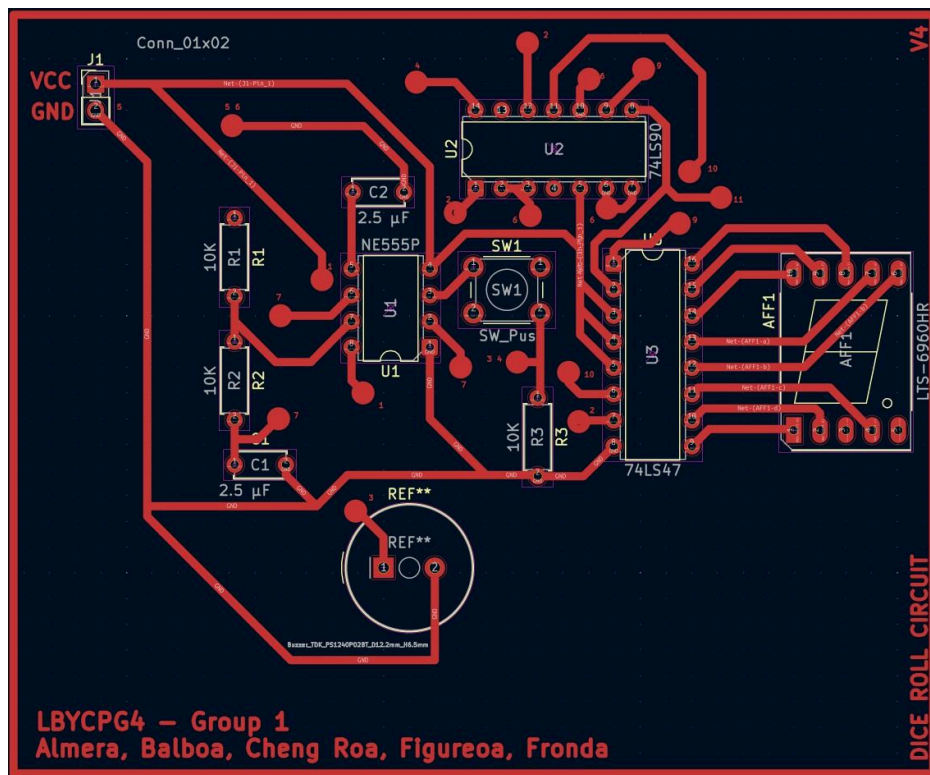


Figure 2. PCB Layout

BREADBOARD AND PCB

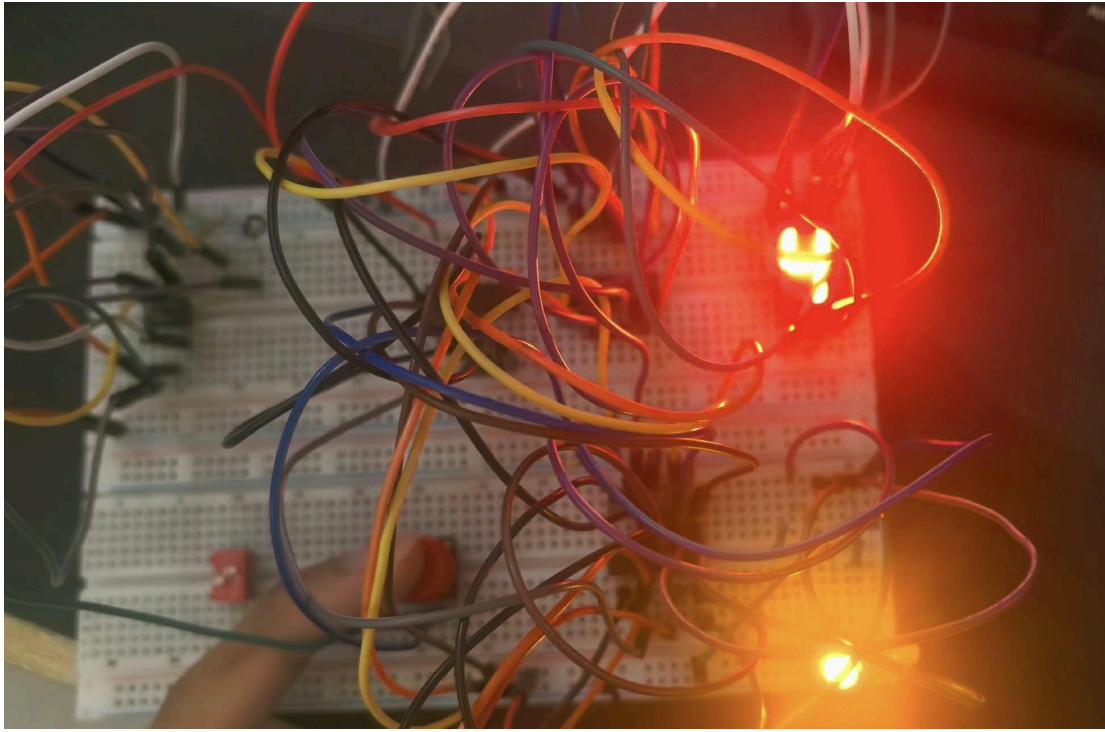


Figure 3. Breadboard Prototype

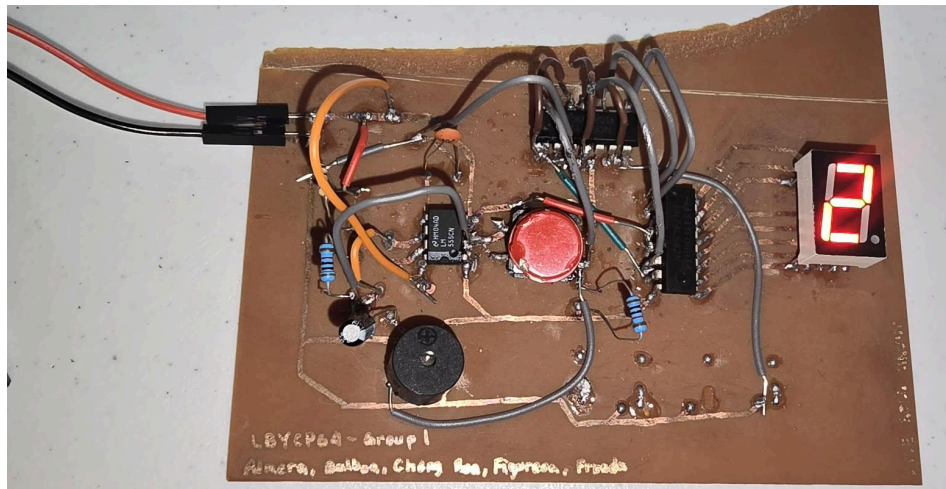


Figure 4. PCB Board

TESTING VERIFICATION

To ensure the design works in real world application, it was first tested using a breadboard before soldering. For its reliability, it was tested in stages of each functionality of the design, the clock pulse generator, BCD counter, and display decoder. With this approach, it allows a find errors in the circuit one by one instead of doing it as a whole, reducing the number of wires needed to be troubleshoot.

Astable 555 Timer

This was the first IC to be connected. It was first configured in astable mode with a large capacitor of 470uF, which is to produce a slow and observable output frequency. A resistor and an LED were connected to the output at Pin 3 to serve as a visual indicator of the pulse.

74LS90 BCD Counter

For its verification, the counting behavior was tested independently using a button, moving it from a manually driven input to a pushbutton tied to Vcc, to see each state, one pulse at a time. LEDs were then connected to the four outputs of the Counter (QA-QD) to monitor the change of each pulse. With each press and release of the button, the sequence 0-9 was observed as well as its rollover to 0. Once confired the clock input was connected to the button whose output was connected in junction with a 10k pulldown resistor and the 74LS90 CLK. This allows it to roll when the button is pressed.

74LS90 BCD Counter

With the counter verified, the 74LS47 decoder was connected along with a 7-segment display to the 74LS90 outputs. Keeping the 555 clock at a slow rate ensures that each state is seen from 0 to 9. Once it was confined, the capacitor was changed from 470uF to 10uF, which allows quick changes of each state to simulate randomness.

DATA AND RESULTS

Astable 555 Timer - Clock Frequency

The 555 timer is configured in astable mode using 2 $10k\Omega$ resistors for R1 and R2, and a $2.5\mu F$ capacitor for C1, which sets the oscillation frequency that drives the counter of 74LS90

Charging Time (High Output):

$$t_1 = 0.693(R_1 + R_2)C = 0.693(10k + 10k)(2.5 \times 10^{-6}) = 34.65ms$$

Discharging Time (Low Output):

$$t_2 = 0.693(R_2)C = 0.693(10k)(2.5 \times 10^{-6}) = 17.33ms$$

Total Period:

$$T = t_1 + t_2 = 34.65ms + 17.33ms = 51.98ms$$

Frequency:

$$f = 1/T = 19.24Hz$$

Duty Cycle:

$$D = t_1/T = 34.65/51.98 \times 100 = 66.7\%$$

The given components yield roughly 19 clocks per second. Since the average human reaction time is around 200ms, this means that during that period, around 4 clock pulses are done, making it almost impossible to predict or time the exact count of the cycle.

74LS90 BCD Counter

The BCD uses its full sequence before rolling over and restarting the cycle.

QD	QC	QB	QA	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3

0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Once the counter reaches the decimal 10 (1010), it automatically resets the counter and repeats the cycle.

74LS47 BCD-to-7-segment Decoder

The QA-QD lines from 74LS90 is feed directly into the 74LS47, which drives the common-anode display. Since the output of the 74LS47 is on active-LOW, a 0 turns on the corresponding segment ON:

QDQCQBQA	a	b	c	d	e	f	g	Display
0000	0	0	0	0	0	0	1	0
0001	1	0	0	1	1	1	1	1
0010	0	0	1	0	0	1	0	2
0011	0	0	0	0	1	1	0	3
0100	1	0	0	1	1	0	0	4
0101	0	1	0	0	1	0	0	5
0110	1	1	0	0	0	0	0	6
0111	0	0	0	1	1	1	1	7
1000	0	0	0	0	0	0	0	8
1001	0	0	0	1	1	0	0	9

The table shows how the BCD output of the 74LS90 has a corresponding and correctly decoded digit on the display, validating that no invalid or black states occur during the counting cycles.

ANALYSIS

The theoretical calculations confirm that the circuit meets its goals of producing an unpredictable output that relies purely on digital logic.

The 555 timer's astable configuration produces a frequency of 19.24Hz with a period of 52ms. This is much faster than the average human reaction time, around 200ms, making sure that the user cannot reliably time their button to land on a specific count, which is the basis for the randomness of its generation.

The 74LS90 truth table confirms that a complete and uniform 10-state BCD cycle (0-9) must be equally likely to be displayed. While the 74LS47 decoding table confirms that every BCD state maps to a valid and correctly illuminated digit.

However, during the breadboard prototype and testing, the display showed a particular bias towards even numbers, which was likely caused by loose connections or contact resistance affecting the edge triggered clock signal. This was resolved after soldering the design onto a PCB, which restored the stable, low-resistance connections and produced an unbiased output distribution. Showing the importance of its connections and how it can affect the performance of its design when created in the physical format.

CONCLUSION

The circuits demonstrate a functional 10-digit random number generator created entirely from IC's and timing components. By making the frequency and period of cycling low, it creates a mismatch between the clock display and human reaction time. This achieves an unpredictable output using just a 555 timer, 74LS90 counter, and 74LS47 decoder. All stages performed within expected, safe parameters, and the even number bias observed on the breadboard, which was resolved through PCB soldering, reinforced the importance of solid physical construction alongside correct theoretical design.

